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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Pierte Roo

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EXAMINER

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/790,689	<b>Applicant(s)</b> ROO, PIERTE	
	<b>Examiner</b> SIU M. LEE	<b>Art Unit</b> 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 March 2010.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-108 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-108 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments, see page 2-8, filed on 3/25/2010, with respect to the rejections of claims 1-108 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wood (US 2003/0006851 A1).

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 8-16, 21-31, 36-38, 42-49, 53-60, 64-67, 72-80, and 85-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (US 6,717,997 B1, hereinafter Cranford) in view of Wood (US 2003/0006851 A1).

(1) Regarding claims 1 and 14:

Cranford discloses a system comprising:

a plurality of information communication device (a plurality of clock generator circuits 510 and transceivers (PHYs) 310 in figure 5, column 6, lines 24-25); wherein each of the of the plurality of information communication devices is responsive to a

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respective information communication clock signal (each of the clock generator circuits 510 and transceivers (PHYs) 310 in figure 5 is response to the respective clock signal (C11 to C1n) from the second phase control circuit 120" as shown in figure 5), and wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (all the phased signal C11 to C1n are associated to the reference clock signal 101 as shown in figure 5); and

a phase controller (phase control circuit 110 and a string of delay elements 120'), wherein the phase controller responsive to the common phase reference clock signal (Reference clock signal 101 that is input to the phase control circuit 110 as shown in figure 5), and wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (the aspect of the invention can provide known, constant phasing between transceiver 310, column 6, lines 37-38, each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39, the examiner interpret the known constant phase difference between the clock signal (C11 to C1n) as a predetermined amount of phase difference).

Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock having a different phase in a clock cycle, the current demand of each transceiver 310

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would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and  $\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$
third I/O latch	$135^\circ$	$315^\circ$
fourth I/O latch	$225^\circ$	$45^\circ$

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
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first I/O latch	315°	135°
second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford to prevent current spike (ground bounce) that cause noise and compromise system performance.

(2) Regarding claims 2 and 15:

Cranford discloses wherein each of the plurality of information communication devices is responsive to the common reference clock signal altered by the phase controller (each of the transceiver (PHYs) 310 is responsive to the phased clock signal C11 to C1n, column 7, lines 14-16, each of the phased clock signal obtained by from

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the reference clock signal altered by the string of delay 120'), and wherein each of the plurality of information communication devices comprises a device clock (clock generator circuit 510 in figure 5) for generating the respective information communication clock signal (C21 to C2m), using the common reference clock signal (the common clock signal 101 is altered by the phase control circuit 110 and a string of delay elements 120' to generate the first plurality of phased clock signals (C11 to C1n), which are in turn provide to a plurality of clock generator circuits 510 that produce a second plurality of phased clock signal C21 to C2m, clock generator circuits 510 may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-13).

(3) Regarding claims 3 and 16:

Cranford discloses wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by the predetermined amount ( each of the C11 to C1n are delay by a delay element D as shown in figure 5) to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39).

(4) Regarding claims 8, 21, 42 and 53:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (120' in figure 5 comprises a plurality of delay elements).

(5) Regarding claims 9, 22, 43 and 54:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, therefore, they are being generated by a plurality of delay locked loops).

(6) Regarding claims 10, 23, 44, and 55:

Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(7) Regarding claims 11, 24, 45, and 56:

Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked

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loops), wherein the at least one delay locked loop is in communication with each of the plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and wherein each information communication channel includes at least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

(8) Regarding claims 12, 25, 46 and 57:

Cranford discloses wherein the information communication system comprises an Ethernet transceiver (fast Ethernet transceiver (FET), column 3, lines 36-39).

(9) Regarding claim 13, 26, 36, 47, 58 and 64:

Cranford discloses wherein the Ethernet transceiver is compliant with I.E.E.E. 802.3ab (a multiport fast Ethernet transceiver (FET) chip implementing a 100Tx(IEEE standard 802.3) class I or in class 2 repeater, column 2, lines 13-15).

(10) Regarding claim 27:

Cranford discloses a method comprising the steps of:

generating an information communication clock signal in each of the plurality of information communication devices (a plurality of clock generator circuits 510 generate a plurality of clock signals (C21 to C2m) for each respective transceivers (PHYs) 310 in figure 5, column 6, lines 24-25),

wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal

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(the signal C21 to C2m are obtain from clocks signal C11 to C1n and all the phased signal C11 to C1n are associated to the reference clock signal 101 as shown in figure 5, therefore the signal C21 to C2m are associated with the reference clock signal 101); and

altering a phase of each information communication clock signal for each of the plurality of information communication devices by a predetermined amount (the second phase control circuit 120", controlled delays can be produces such that the phased output signals C11 to C1n are phased with respect to one another by time intervals that are on the order of nanoseconds, column 4, lines 56-60, these delay circuit can be used to generate precisely phased control signal for operating the components, column 2, lines 57-67 ,the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39, the examiner interprets the known and constant phase amount as a predetermined amount).

Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock having a different phase in a clock cycle, the current demand of each transceiver 310 would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and  $\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$
third I/O latch	$135^\circ$	$315^\circ$
fourth I/O latch	$225^\circ$	$45^\circ$

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$

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third I/O latch	135°	315°
fourth I/O latch	225°	45°

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford to prevent current spike (ground bounce) that cause noise and compromise system performance.

(11) Regarding claim 28:

Cranford discloses the method further comprising the step of receiving the common reference clock signal in each of the plurality of information communication devices (as shown in figure 1, each phase control circuit 120 receives the input control signal 103).

(12) Regarding claim 29:

Cranford discloses wherein the method further comprising the step of generating each information communication clock signal for each of the plurality of information communication devices using the common reference clock signal (the second phase control circuit 120 are configured to receive input control signals 130 and operative to generate phased output control signals 121 that are phased dependent upon the applied phase control signal 113, column 4, lines 33-37, the second phase control circuit 120, controlled delays can be produces such that the phased output signals 121 are phased with respect to one another by time intervals that are on the order of nanoseconds).

(13) Regarding claim 30:

Cranford discloses the step of altering the phase of the common reference clock signal for each of the plurality of information communication devices by the predetermined amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (figure 5 discloses another embodiment of that the common reference clock signal (103) is being phase shifted for each of the information communication devices (clock generating circuit 510 and PHY 310) by a known amount, such that each phase clock signal C11 to C1n have a known phase difference, thus makes each of the second phased clock signal C21 to C2m have the same known phase different between one another, column 7, lines 1-16).

(14) Regarding claim 31:

Cranford discloses the step of time delaying the common reference clock signal supplied to each of the plurality of information communication devices by the predetermined amount (a string of delay element D in 120' produce a first plurality of phased clock signal C11 to C1n, each of the multi-phased clock signal can provide known, constant phasing between the PHYs 310, since the phase clock signals have a constant phase difference between each other, therefore, each of them is being time delay with the same amount relatively to each other, figure 5)

(15) Regarding claims 37 and 48:

Cranford discloses a system comprising:

a plurality of information communication devices (a plurality of transceivers (PHYs) 310 in figure 5, column 6, lines 24-25),

wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal (a plurality of clock generator circuits 510 generate a plurality of clock signals (C21 to C2m) for each respective transceivers (PHYs) 310 in figure 5, column 6, lines 24-25),

wherein each of the plurality of information communication devices is responsive to a common reference clock signal (each information communication device is responsive to the clock signal C21 to C2m wherein C21 to C2m are obtain from clocks signal C11 to C1n and all the phased signal C11 to C1n are associated to the reference clock signal 101 as shown in figure 5, therefore the information communication device PHY 310 are associated with the reference clock signal 101),

wherein the information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal (the signal C21 to C2m are obtain from clocks signal C11 to C1n and all the phased signal C11 to C1n are associated to the reference clock signal 101 as shown in figure 5, therefore the signal C21 to C2m are associated with the reference clock signal 101); and

a phase controller (phase control circuit 110 and a string of delay elements 120'), wherein the phase controller is responsive to the common reference clock signal (the first phase control circuit 110 including ring oscillator circuit 114 including a first string of delay circuit D that produce an output signal 111 that is phase locked to a reference clock signal 101 through the action of a loop control circuit 112 based on a comparison of the reference clock signal 101 and the output signal 111, column 4, line 65 – column 5, line 4), and

wherein the phase controller alters a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount to alter a phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (the aspect of the invention can provide known, constant phasing between transceiver 310, column 6, lines 37-38, each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39, the examiner interpret the known constant phase difference between the clock signal (C11 to C1n) as a predetermined amount of phase difference).

Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock having a different phase in a clock cycle, the current demand of each transceiver 310 would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and  $\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$

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second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	315°	135°
second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford to prevent current spike (ground bounce) that cause noise and compromise system performance.

(16) Regarding claims 38 and 49:

Cranford discloses wherein each of the plurality of information communication devices comprises a device clock for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (each transceiver 310 has a clock generator circuit 510 that may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-12, figure 5).

(17) Regarding claim 59:

Cranford discloses a method comprising the steps of:

receiving a common reference clock signal (Reference clock signal 101 as shown in figure 5),

wherein each of the plurality of information communication device is responsive to the common reference clock signal (each information communication device is responsive to the clock signal C21 to C2m wherein C21 to C2m are obtain from clocks signal C11 to C1n and all the phased signal C11 to C1n are associated to the reference clock signal 101 as shown in figure 5, therefore the information communication device PHY 310 are associated with the reference clock signal 101);

altering a phase of the common reference clock signal for each of the plurality of information communication devices by a predetermined amount (a string of delay element 120" in figure 5 producing a plurality of phased clock signal C11 to C1n, column 7, lines 1-3, the multi-phase clock signal C11 to C1n according to this aspect of invention can provide known, constant phasing between the transceivers 310, column 6,

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lines 36-38, the examiner interprets the known and constant phasing as a predetermined amount of phase shift); and

generating an information communication clock signal for each of the plurality of information communication devices using common reference clock signal that was phase altered (the first phased clock signals C11 to C1n (phase altered reference clock signal) are in turn provided to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signals C21 to C2m for the respective PHY 310 as shown in figure 5, column 7, lines 3-6);

wherein a phase of each information communication clock signal of each of the plurality of information communication devices is altered by the predetermined amount (a input clock signal 103 is provide to a string of delay element 120" producing a plurality of phased clock signal C11 to C1n, column 7, lines 1-3, the multi-phase clock signal C11 to C1n according to this aspect of invention can provide known, constant phasing between the transceivers 310, column 6, lines 36-38, the examiner interprets the known and constant phasing as a predetermined amount of phase shift and the phased clock signal C11 to C1n are provide to the clock generator circuit 510 wherein the clock generator circuit 510 as clock division to support multi-speed protocols, column 7, lines 10-12, since the C11 to C1n are separate by a constant phase difference, therefore, after the processing of the clock generator circuit 510 such as frequency division, the clock signals C21 to C2m will maintain the phase difference in clock signals C11 to C1n).

Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock having a different phase in a clock cycle, the current demand of each transceiver 310 would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and  $\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$

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second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	315°	135°
second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford to prevent current spike (ground bounce) that cause noise and compromise system performance.

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(18) Regarding claim 60:

Cranford discloses wherein the step of altering comprising the step of:

time delaying the common reference clock signal supplied to each of the plurality of information communication devices by the predetermined amount ((a input clock signal 103 is provide to a string of delay element 120” producing a plurality of phased clock signal C11 to C1n, column 7, lines 1-3, the multi-phase clock signal C11 to C1n according to this aspect of invention can provide known, constant phasing between the transceivers 310, column 6, lines 36-38, the examiner interprets the known and constant phasing as a predetermined amount of phase shift).

(19) Regarding claims 65 and 78:

Cranford discloses a device comprises:

a plurality of transceivers (a plurality of clock generator circuit 510 and transceivers (PHYs) 310 in figure 5, column 6, lines 24-25), wherein each of the plurality of transceivers comprising:

a plurality of information communication devices (receiver 312 and transmitter 314 in each of the transceiver 310 as shown in figure 4);

wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal ((the first plurality of phased clock signals C11 to C1n are in turn provided to a plurality of clock generating circuits 510 that produce a second plurality of phased clock signal C21 to C2m that supply to the plurality of transceiver PHYs 310, column 7, lines 3-6, the phased clock signals are for driving the transceiver, column 2, lines 51-54);

wherein each information communication clock signal of each of the plurality of information communication devices is associated with a common reference clock signal (each of the clock signals C21 to C2m are associated to the phased clocks signal C11 to C1n and all the phased clock signal C11 to C1n are associated with the output clock signal 103 as shown in figure 5, column 4, line 65 – column 5, lines 4); and

a phase controller (phase control circuit 110 and a string of delay elements 120' in figure 5),

wherein the phase controller is responsive to the common reference clock signal (the phase control circuit 110 synchronizes a clock signal 111 produced by a clock generator circuit 510 that receives the output signal 103 produce by phase control circuit 110 to a reference signal 101, column 7, lines 6-10), and

wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (these delay circuit can be used to generate precisely phased control signal for operating the components, column 2, lines 57-67 ,the multi-phase clock signal according to this aspect of the present invention can provide known, constant phasing between the transceiver 310, column 6, lines 36-39, the examiner interpret known, constant phase shift as a predetermined phase altering).

Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock

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having a different phase in a clock cycle, the current demand of each transceiver 310 would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and  $\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$
third I/O latch	$135^\circ$	$315^\circ$
fourth I/O latch	$225^\circ$	$45^\circ$

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

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I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	315°	135°
second I/O latch	45°	225°
third I/O latch	135°	315°
fourth I/O latch	225°	45°

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford to prevent current spike (ground bounce) that cause noise and compromise system performance.

(20) Regarding claim 66 and 79:

Cranford discloses wherein each of the plurality of information communication device is responsive to the common reference clock signal altered by the phase controller (the output signal of the phase control circuit is being phase delay by 102° and

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then provided to the plurality of clock generating circuit 510 to generate the phased clock signal C21 to C2m to drive the transceiver (PHYs) 310), and wherein each of the plurality of information communication devices comprises a device clock (clock generating circuit 510) for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (each transceiver 310 has a clock generator circuit 510 that may implement a variety of clock processing functions, such as clock division to support multi-speed protocols, column 7, lines 10-12, figure 5).

(21) Regarding claims 67 and 80:

Cranford discloses wherein the phase controller (phase control circuit 110 and a string of delay elements 120') alters a phase of the common reference clock signal for each of the plurality of information communication devices (C11 to C1n are phase alter by the delay D in the phase control circuit 120' as shown in figure 5) by the predetermined amount (each of the phase signal C11 to C1n are different by a delays D as shown in figure 5, the examiner interpret known, constant phase shift as a predetermined phase altering) to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (the phased clock signal C11 to C1n are provide to the clock generator circuit 510 wherein the clock generator circuit 510 as clock division to support multi-speed protocols, column 7, lines 10-12, since the C11 to C1n are separate by a constant phase difference, therefore, after the processing of the clock generator circuit

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510 such as frequency division, the clock signals C21 to C2m will maintain the phase difference in clock signals C11 to C1n).

(22) Regarding claims 72 and 85:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (a string of time delay elements D in 120' in figure 5, column 7, lines 1-2).

(23) Regarding claims 73 and 86:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops).

(24) Regarding claims 74 and 87:

Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(25) Regarding claims 75 and 88:

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Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops), wherein the at least one delay locked loop is in communication with each of the plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and wherein each information communication channel includes at least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

(26) Regarding claim 76 and 89:

Cranford discloses the number of plurality of transceiver equal to  $n+1$ .

Cranford is silent about the exact number of transceiver comprise one of four or eight. However, since  $n$  is a variable is there is no constrain on what  $n$  can be equal to, it would have been obvious that  $n$  can be equal to 3 or 7, thus make the number of transceiver equal to one of four or eight.

(27) Regarding claim 77 and 90:

Cranford discloses wherein each of the plurality of transceiver comprises an Ethernet transceiver (fast Ethernet transceiver (FET), column 3, lines 36-39).

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(28) Regarding claims 5, 18, 33, 40, 51, 62, 69, and 82:

Cranford and Wood disclose all subject matter in claims 1, 14, 27, 37, 48, 59, 65, 78 and Cranford further discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information communication devices by a known and constant amount and Wood further disclose in figure 32a that each data latch 84 of the IC 68<sub>1</sub> or 68<sub>2</sub>, the phase of the transmit clock signals have a phase difference of 90 degrees (45, 135, 225, 315).

It is desirable to have the known and constant amount is 90 degrees because it spreads out the dynamic transient current drawn and reduces the ground bounce by a factor of four. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the known and constant amount as 90 degrees as taught by Wood in the system and method of Cranford to reduce the dynamic transient current drawn and improve the performance.

4. Claims 91-93, 96-102, and 105-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Watanabe et al. (US 2003/0197498 A1) and Wood (US 2003/0006851 A1).

(1) Regarding claim 91 and 100:

Cranford discloses a system comprising:

a plurality of information communication devices (transceiver (PHYs) 310),

wherein each of the plurality of information communication devices is responsive to the common reference clock signal (the phase control signal generated by the phase-

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lock loop circuit is applied to a string of delay circuits that produce a plurality of phased output signals C11 to C1n that are process by the clock generator circuit 510 to generate the clock signals C21 to C2m that is used to drive a plurality of PHYs 310 as shown in figure 5, column 2, lines 51-54, column 6, line64 – column 7, line16),

wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal (the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, column 7, lines 3-6),

wherein each information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal (the output signal 103 provided to a string of delay 120' to generate a first plurality of phased clock signal and then the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, therefore the each information communication clock signal of each of the plurality of information communication devices is associated with the common reference clock signal 103, column 7, lines 1-22); and

a phase controller (phase control circuit 110 and string of delay element 120'),

wherein the phase controller is responsive to the common reference clock signal (delay element is operative to produced phased output control signals from at least one input control signal responsive to the phase control signal, column 2, lines 43-46),

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wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount (a string of delay elements D 120' produce phased clock signals C11 to C1n from an input clock signal 103 responsive to phase control signal 113, the multi-phase clock signals C11 to C1n can provide known, constant phasing between the transceiver 310, column 6, lines 36-39, the examiner interprets the known and constant phase shift amount as a predetermined phase shift amount), and

wherein each of the plurality of information communication devices comprises a device clock for generating the respective information communication clock signal using the common reference clock signal altered by the phase controller (the first plurality of phased clock signal C11 to C1n are in turn provide to a plurality of clock generator circuit 510 that produce a second plurality of phased clock signal C21 to C2m to drive the PHYs 310, column 7, lines 3-6).

Cranford discloses a reference clock signal input to the phase control circuit 110 but fails to explicitly disclose (a) a reference clock generator for generating the common reference clock signal; and (b) the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

With respect to (a), Watanabe et al. disclose a reference clock generator for generating a common reference clock signal (reference clock generator 10 generating the reference clock MCK, paragraph 3-5).

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It is desirable to use a reference clock signal generator for generating the common reference clock signal because it provides a stable clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Watanabe et al. in the system of Cranford to increase the stability of the system.

With respect to (b), Cranford discloses a plurality of transceiver 310 in figure 5 that each of the transceivers is driven by a clock with a particular phase shift with respect to the other clocks (each information communication clock signal C11 to C1n is being delay by delay element D in 120", column 6, lines 31-39). As each transceiver is driven by a clock having a different phase in a clock cycle, the current demand of each transceiver 310 would have a different phase, therefore, the summation of current demand of all transceivers 310 would have a current demand spread out over a period of time.

Cranford discloses the multi-phase clock signal generated by the phase controller circuit 110 can provide known constant phasing between the transceiver (column 6, lines 35-39) but fails to explicitly disclose the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.

However, Wood discloses a circuit (figure 32a) that comprises a plurality of I/O latch 84 (detail of latch as shown in figure 32b), the I/O latch in the right column belongs to a monolithic IC 68<sub>1</sub> and the I/O latch in the left column belongs to monolithic IC 68<sub>2</sub>. Each I/O latch is driven by a transmit clock and a receive clock with phase of  $\Phi 1$  and

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$\Phi 2$  respectively and a phase difference of  $180^\circ$  between  $\Phi 1$  and  $\Phi 2$  as shown in figure 32b.

As shown in figure 32a, the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the right column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$
third I/O latch	$135^\circ$	$315^\circ$
fourth I/O latch	$225^\circ$	$45^\circ$

and the phase of  $\Phi 1$  and  $\Phi 2$  of each I/O latch in the left column are as following:

I/O latch	$\Phi 1$	$\Phi 2$
first I/O latch	$315^\circ$	$135^\circ$
second I/O latch	$45^\circ$	$225^\circ$
third I/O latch	$135^\circ$	$315^\circ$
fourth I/O latch	$225^\circ$	$45^\circ$

From the above table, we can see that phase of  $\Phi 1$  and  $\Phi 2$  of the I/O latch in the left and right column is the same, that is the transmission and receiving activity of I/O latch in the left and right column is trigger at the same time. Therefore, combined amplitude of waveform of output current of each pair of I/O latch in the left column and the right column is at least double of individual waveform of each output current event of each I/O latch (paragraph 0150 – 0154).

It is desirable to have the phase shift by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices because it reduces ground bounce and positive supply voltage dips (paragraph 0153). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Wood in the system and method of Cranford and Watanabe et al. to prevent current spike (ground bounce) that cause noise and compromise system performance.

(2) Regarding claims 92 and 101:

Cranford discloses wherein the phase controller (phase control circuit 110 and 120' in figure 5) alters a phase of the common reference clock signal (the output signal 103 of phase control circuit 110) for each of the plurality of information communication devices (C11 to C1n are each different by a known amount of phase shift) by the predetermined amount to alter the phase of each information communication clock signal of each of the plurality of information communication devices by the predetermined amount (the multi-phase clock signals C11 to C1n is use to drive the transceiver PHYs 310 and each of them is different by a known amount of phase shift, column 6, lines 36-39, a string of delay elements D 120' produce phased clock signals C11 to C1n from an input clock signal 103 responsive to phase control signal 113, the multi-phase clock signals C11 to C1n can provide known, constant phasing between the transceiver 310, column 6, lines 36-39, the examiner interprets the known and constant phase shift amount as a predetermined phase shift amount, since the C11 to C1n are separate by a constant phase difference, therefore, after the processing of the clock

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generator circuit 510 such as frequency division, the clock signals C21 to C2m will maintain the phase difference in clock signals C11 to C1n).

(3) Regarding claims 93 and 102:

Cranford discloses wherein the phase controller alters the phase of each information communication clock signal of each of the plurality of information communication devices by a known and constant amount.

Cranford does not explicitly disclose that the known and constant amount is 90 degrees.

Although Cranford does not specifically disclose wherein the known and constant amount is 90 degrees, such limitation are merely a matter of design choice and would have been obvious in the method of Cranford. Cranford teaches the altering of the phase of each information communication clock signal of each of the plurality of information communication devices by a known and constant amount. The limitation of the known and constant amount is 90 degrees do not define a patentably distinct invention over Cranford since both invention as a whole are directed to avoid electromagnetic interference due to unwanted transient in the supply voltage and current (current spike associated with increased instantaneous current demand can cause noise that can compromise system performance, column 1, lines 50-52). Therefore, the known and constant amount is 90 degrees would have been a matter of obvious design choice to one of ordinary skill in the art.

(4) Regarding claims 93 and 102:

Wood further disclose in figure 32a that each data latch 84 of the IC 68<sub>1</sub> or 68<sub>2</sub>, the phase of the transmit clock signals have a phase difference of 90 degrees (45, 135, 225, 315).

It is desirable to have the known and constant amount is 90 degrees because it spreads out the dynamic transient current drawn and reduces the ground bounce by a factor of four. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the known and constant amount as 90 degrees as taught by Wood in the system and method of Cranford and Watanabe et al. to reduce the dynamic transient current drawn and improve the performance.

(5) Regarding claims 96 and 105:

Cranford discloses wherein the phase controller comprises a plurality of time delay elements (a string of time delay elements D in 120' in figure 5, column 7, lines 1-2).

(6) Regarding claims 97 and 106:

Cranford discloses wherein the plurality of time delay elements comprises a plurality of delay locked loops (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops).

(7) Regarding claims 98 and 107:

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Cranford discloses wherein the plurality of time delay elements are arranged in cascade (120' in figure 5 comprises a cascade of delay elements), and wherein each of the plurality of information communication devices is in communication with at least one of the plurality of time delay elements (each of the transceivers (PHYs) 310 is connected to a first phased clock signals C11 to C1n produce by the delay element strings in 120' as shown in figure 5).

(8) Regarding claims 99 and 108:

Cranford discloses wherein the phase controller further comprises at least one delay locked loop (each of the phased control signal C11 to C1n are generated by a string of delay element, a output signal 103 produced by the phase control circuit 110 to a reference clock signal 101, and a phase control signal 113, therefore, for each of the phase control signal, it is being generated by a delay locked loop and for all the phased control signal C11 to C1n, they are being generated by a plurality of delay locked loops),

wherein the at least one delay locked loop is in communication with each of the plurality of information communication devices via an information communication channel (each of the phased clock signal is communicated with its respective transceiver 310), and

wherein each information communication channel includes at least one of the plurality of time delay elements (each of the phased clock signal would pass through at least one delay element (delay element in 114 and delay element in 120') of the phase controller).

5. Claims 4, 17, 32, 39, 50, 61, 68, 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Wood (US 2003/0006851 A1) as applied to claims 1, 14, 27, 37, 48, 59, 65, 78 above, and further in view of Watanabe et al. (US 2003/0197498 A1).

Cranford and Wood disclose all subject matter as discussed in claims 1, 14, 27, 37, 48, 59, 65, 78 and Cranford further disclose a reference clock signal input to the phase control circuit 110 but fails to explicitly disclose a reference clock generator for generating the common reference clock signal.

However, Watanabe et al. disclose a reference clock generator for generating a common reference clock signal (reference clock generator 10 generating the reference clock MCK, paragraph 3-5).

It is desirable to use a reference clock signal generator for generating the common reference clock signal because it provides a stable clock signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Watanabe et al. in the system of Cranford and Wood to increase the stability of the system.

6. Claims 7, 20, 34, 71, and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Wood (US 2003/0006851 A1) as applied to claims 1, 14, 27, 65, 78 above, and further in view of Ishikawa et al. (US 5,610,911).

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Cranford and Wood disclose all subject matter as discussed in claims 1, 14, 27, 65, 78 and Cranford discloses the phase controller comprises a phase locked loop (first phase control circuit 110 in figure 5, a first phase control circuit, e.g. a phase locked loop is operative to synchronize an output signal thereof through intermediate generation of a phase control signal, column 2, lines 39-43).

Cranford and Wood disclose all the subject matter as discuss in claims 7, 20, 34, 71, and 84 except a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop, wherein the output signal is associated with the information communication clock signal, and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices.

However, Ishikawa et al. discloses the using of a sync signal phase control 14 in figure 3 to control the resetting time of the frequency divider 13 in order to change the phase of the output signal of the frequency divider (column 5, lines 55-column 6, 24, column 13, lines 4-7, 26-37, column 16, lines 20-31).

It is desirable to use a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication

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devices because it provides a simple circuit for generating a plurality of phased clock signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to combine the PLL of Cranford and Wood with the sync signal phase control 14 and frequency divider 13 of Ishikawa et al. to generate a plurality of phased clock signal for each of he plurality of information communication devices so as to reduce the complexity of the system.

7. Claims 6, 19, 35, 41, 52, 63, 70, and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Wood (US 2003/0006851 A1) as applied to claims 1, 14, 27, 37, 48, 59, 65, 78 above, and further in view of Graef (European Patent Application EP 0 903 660 A1).

Cranford and Wood disclose all subject matter as discussed in claims 1, 14, 27, 37, 48, 59, 65, and 78 except wherein the phase of at least two of the information communication clock signals are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system.

However, Graef discloses a clock distribution system (system in figure 6 and 7) that wherein the phase of at least two of the information communication clock signals are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system (in figure 6, the

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clock distribution network 200 includes at least buffers or drivers 210, 212, and 214 formed on the substrate 202 for causing the clock signal to have a relative phase of  $\Phi_0$ ,  $\Phi_1$ , and  $\Phi_2$  at the input of clock trees 204, 206, and 208, figure 7 shows an embodiment of the clock tree that contains a buffer or driver element 320 on one side of the clock tree, thus generating a different phase for the buffer clock recipient fan-out 304c and 304d, and the buffer clock recipient fan-out 304 and 304b receiver a clock with different phase, when using the clock tree of figure 7 in the clock distribution system in figure 6, each clock tree would have 2 buffer clock recipient fan-out receive a same clock with a first phase and the other two buffer clock recipient fan-out would receive another clock with different phase, with the total of 3 clock trees as shown in figure 6, there will be 6 different phase clock signals in total and 2 buffer clock recipient fan-out of a clock tree will share a same phase clock signal, page 7, paragraph 0048 – page 8, paragraph 0050.)

It is desirable to have the phase of at least two of the information communication clock signals are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system because this result in a reduction in the adverse effect of ground bounce and  $V_{DD}$  noise (paragraph 0050, lines 52-53). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Graef in the method and system of Cranford and Wood to reduce the effect of ground bounce.

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8. Claims 95 and 104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Watanabe et al. (US 2003/0197498 A1) and Wood (US 2003/0006851 A1) as applied to claims 91 and 100 above, and further in view of Ishikawa et al. (US 5,610,911).

Cranford discloses the phase controller comprises a phase locked loop (first phase control circuit 110 in figure 5, a first phase control circuit, e.g. a phase locked loop is operative to synchronize an output signal thereof through intermediate generation of a phase control signal, column 2, lines 39-43).

Cranford, Watanabe et al. and Wood disclose all the subject matter as discuss in claims 91 and 100 except a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of signal division of an output signal of the phase locked loop, wherein the output signal is associated with the information communication clock signal, and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices.

However, Ishikawa et al. discloses the using of a sync signal phase control 14 in figure 3 to control the resetting time of the frequency divider 13 in order to change the phase of the output signal of the frequency divider (column 5, lines 55-column 6, 24, column 13, lines 4-7, 26-37, column 16, lines 20-31).

It is desirable to use a signal division controller in communication with the phase locked loop, wherein the signal division controller is configured to control a start time of

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signal division of an output signal of the phase locked loop and wherein the start time of signal division of the output signal is varied to alter the phase of each information communication clock signal of each of the plurality of information communication devices because it provides a simple circuit for generating a plurality of phased clock signal. Therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to combine the PLL of Cranford, Watanabe et al. and Wood with the sync signal phase control 14 and frequency divider 13 of Ishikawa et al. to generate a plurality of phased clock signal for each of he plurality of information communication devices so as to reduce the complexity of the system.

9. Claims 94, and 103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (Cranford) (US 6,717,997 B1) in view of Watanabe et al. (US 2003/0197498 A1) and Wood (US 2003/0006851 A1) as applied to claims 91 and 100 above, and further in view of Graef (European Patent Application EP 0 903 660 A1).

Cranford, Watanabe et al. and Wood discloses all subject matter as discussed in claims 91 and 100 except wherein the phase of at least two of the information communication clock signals are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system.

However, Graef discloses a clock distribution system (system in figure 6 and 7) that wherein the phase of at least two of the information communication clock signals

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are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system (in figure 6, the clock distribution network 200 includes at least buffers or drivers 210, 212, and 214 formed on the substrate 202 for causing the clock signal to have a relative phase of  $\Phi_0$ ,  $\Phi_1$ , and  $\Phi_2$  at the input of clock trees 204, 206, and 208, figure 7 shows an embodiment of the clock tree that contains a buffer or driver element 320 on one side of the clock tree, thus generating a different phase for the buffer clock recipient fan-out 304c and 304d, and the buffer clock recipient fan-out 304 and 304b receiver a clock with different phase, when using the clock tree of figure 7 in the clock distribution system in figure 6, each clock tree would have 2 buffer clock recipient fan-out receive a same clock with a first phase and the other two buffer clock recipient fan-out would receive another clock with different phase, with the total of 3 clock trees as shown in figure 6, there will be 6 different phase clock signals in total and 2 buffer clock recipient fan-out of a clock tree will share a same phase clock signal, page 7, paragraph 0048 – page 8, paragraph 0050.)

It is desirable to have the phase of at least two of the information communication clock signals are substantially identical, and wherein a number of information communication clock signals with substantially identical phase is less than a total number of information communication clock signals of the information communication system because this result in a reduction in the adverse effect of ground bounce and  $V_{DD}$  noise (paragraph 0050, lines 52-53). Therefore, it would have been obvious to one

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of ordinary skill in the art at the time of invention to employ the teaching of Graef<sup>1</sup> in the method and system of Cranford, Watanabe et al. and Wood to reduce the effect of ground bounce.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Examiner, Art Unit 2611  
6/8/2010

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